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75-GHz SiGe Heterojunction Bipolar Transistors: GaAs Performance in Si Technology?

J. M. C. Stork, J. H. Comfort, G. L. Patton, E. F. Crabbé, and B. S. Meyerson

IBM T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598

Abstract

SiGe HBTs have demonstrated new device and circuit records, extending the speed of silicon bipolar devices closer to a regime dominated by GaAs and other compound semiconductor technologies. This paper gives a review of recent results and describes our present understanding in order to address the potential merits of SiGe HBTs as an extension to Si bipolar technology.

Device Performance

The record breaking cut-off frequency results of SiGe and Si epitaxial base transistors (cf. Figs. 1 and 2) demonstrates the performance potential of Si profile and SiGe bandgap engineering (1). As can be seen in Fig.3, the combination of an thin epitaxial base and shallow polysilicon emitter technology allows sub 50 nm base widths with low base resistance and acceptable breakdown voltages. The base doping at the emitter-base and base-collector junctions is reduced to lower the electric field at the junction, and thus succeeds in improving the leakage and breakdown characteristics. The retrograded base profile at the emitter-base transition would degrade performance in Si-only devices, due to the reverse built-in field, retarding the electron flow. However, the Ge is used to overcome this profile induced field by grading the bandgap across the neutral base. The field induced by the bandgap grading of the Ge (see Fig. 4) increases the velocity of electrons through the base, reducing the base transit time component of the intrinsic profile delay according to (2)

$$\frac{\tau_b \, (SiGe)}{\tau_b \, (Si)} \simeq \frac{2kT}{\Delta E_{gG}} \left(1 - \frac{kT}{\Delta E_{gG}} \right) \qquad (1)$$

where ΔE_{gG} is the bandgap grading across the heavily-doped portion of the neutral base profile. Figure 5 shows the calculated transit time components for a retrograde base profile, with and without SiGe. As a result of the simultaneous reduction in both base transit time and base-emitter junction capacitance, very high frequency response is obtained even at moderate current densities (see also the data in Fig. 1).

The Lightly Doped Collector has been shown (3) to improve the impact ionization breakdown of the base-collector junction without penalty on current density capability and cut-off frequency. As the electric field is more uniformly distributed across the junction region, the average velocity remains high, but the energy the carriers acquire from the field is reduced. An adequate description of the average energy can be obtained from the energy balance equation directly using the following simplifying assumptions (4): heat flow is neglected and kinetic energy is assumed to be negligible compared to the thermal energy. If it is further assumed that the energy relaxation length λ_w is constant, the second-order moment of the Boltzmann equation can be solved explicitly for the average energy as a convolution of the electric field and the exponential decay length λ_w as

$$W(x) - W_o = \frac{3}{5} q \int_0^x F(\zeta) \exp \left(\frac{(\zeta - x)}{\lambda_w} \right) dx \qquad (2)$$

where F is the electric field and $W_o = (3/2)kT_o$ the energy at thermal equilibrium. Although the average energy is not a perfect representation of the energy of the hottest electrons responsible for impact

ionization, it gives an adequate prediction of the breakdown voltage as shown in Fig. 6. Because the maximum carrier energy is located deep inside the base-collector junction, the multiplication factor of Si and SiGe-base devices is essentially equal (cf. Fig. 7). Any difference in breakdown voltage is only due

Table 1

	SI	SIGe
$A_E(\mu m^2)$	0.6x4.3	0.6x4.3
f_T (GHz)	29	50
$R_{bi}(k\Omega/b)$	3.8	8
R_{bx} (Ω)	60	60
R_E (Ω)	18	8
BV_{CEO} (V)	2.4	3.2
BV_{CBO} (V)	11	11
$C_{CB,in}$ (fF/μm^2)	1.7	1.6
$C_{CB,ext}$ (fF/μm^2)	0.9	0.9
C_{EB} (fF/μm^2)	7.8	6.3

Table 1 (ref 5)
Summary of device parameters of circuit transistors

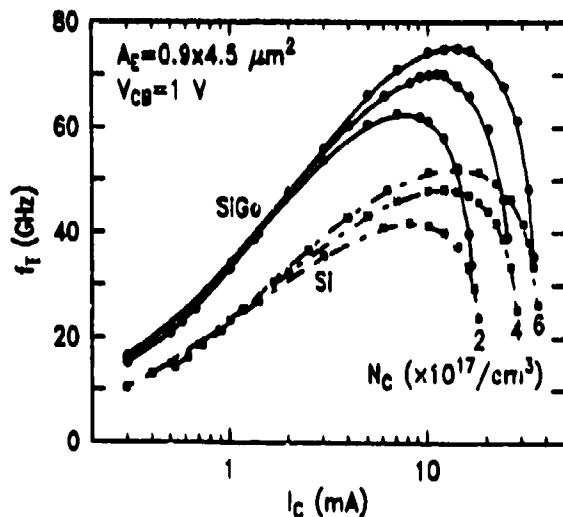**Figure 1** (ref 1)
Measured cut-off frequency versus collector current, for Si and SiGe devices, showing the dependence on collector doping level.
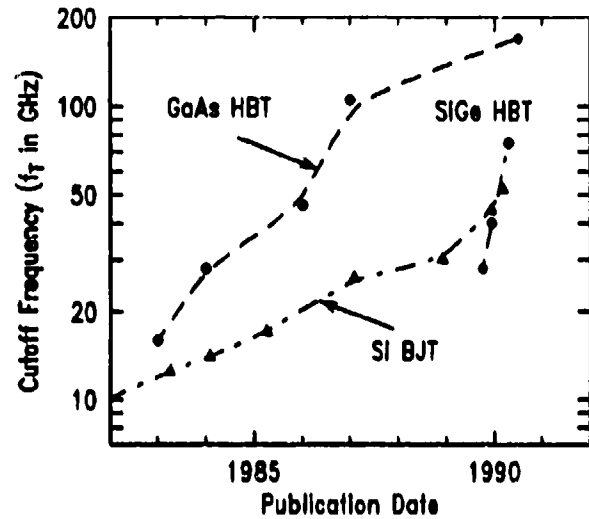

Figure 2
Reported cut-off frequency records in the past decade (at RT). A rapid increase in Si and SiGe performance is apparent.
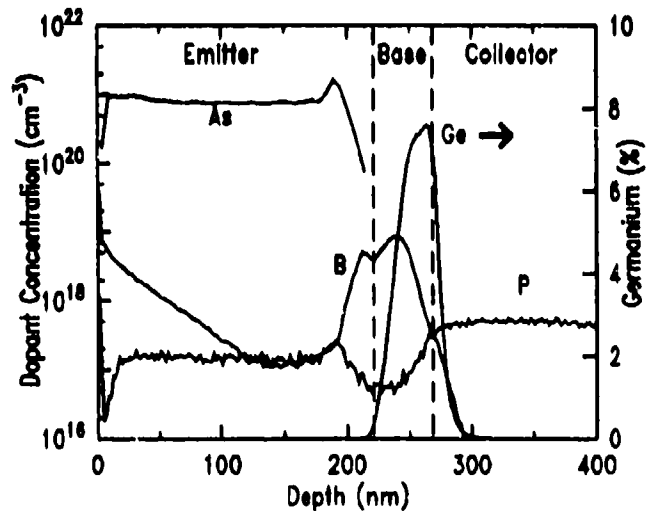

Figure 3 (ref 1)
SIMS profile for the SiGe-base transistors of Fig.1. The Ge grading is positioned precisely in the most heavily doped region of the base to enhance the base transit time.

to the usually higher gain of the SiGe transistors. The net effect of reduced base transit time, nearly equal (BV_{cbo}) or better (BV_{ebo}) breakdown characteristics compared to Si-only devices, presents a significant paradigm shift of conventional breakdown-speed trade-off as shown in Fig 7.
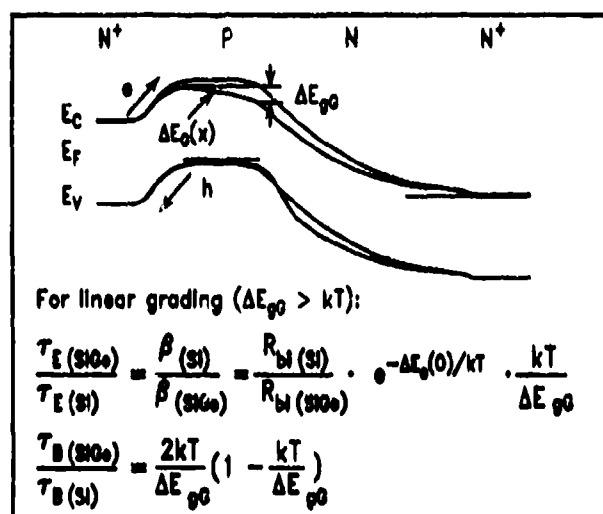
Figure 4 (ref 2)

Energy band diagram illustrating first-order design equations for graded-SiGe-base enhancements in gain and transit times.

Figure 6 (ref 4)

Base-collector voltage at which the base current reverses as a function of collector doping. The insertion of an 1-layer increases the breakdown voltage by 0.3-0.5 Volt.
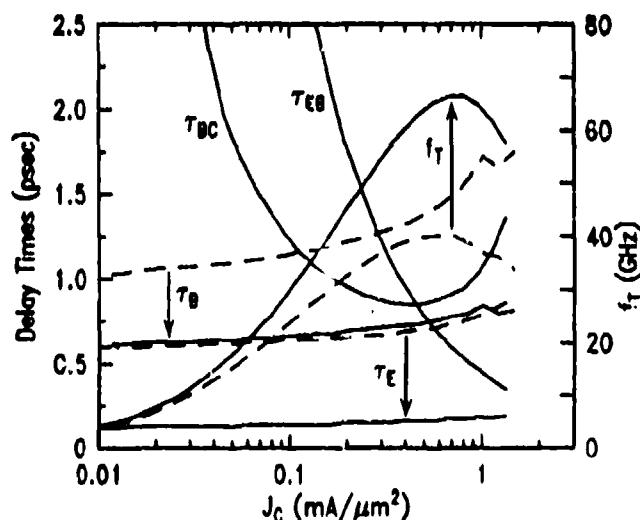

Figure 5 (ref 9)

Calculated transit time components for Si (dashed) and SiGe (solid) profiles showing reduction in both τ_e and τ_b due to the graded Ge profile.

Digital Circuit Performance

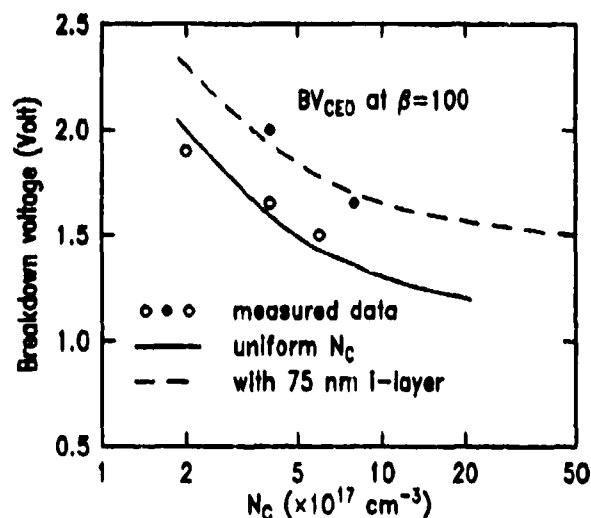Recently, the first circuit results using self-aligned SiGe-base transistors (5 and 6) established new

world records (cf. Fig. 9) and demonstrated a 13% circuit speed improvement in a direct comparison with Si-base devices (cf. Fig. 10). The SiGe profile was designed to produce transistors with $f_T =$ 50 GHz (50 % higher than the 30 GHz for Si) and keep the collector capacitance low for better circuit performance (see Table 1 for a summary of the Si and SiGe device characteristics). The following general relationship for the delay of a current switch (7) can be used to understand the device optimization trade-off's for circuit performance:

$$\tau_d \propto \sqrt{\frac{(2 \times R_b + R_L)(2 \times C_{bc} + C_L)}{2\pi f_T}} \qquad (3)$$

where f_T, R_b, and C_{bc} are the cut-off frequency, base resistance, and collector-base capacitance respectively. For an ECL gate with emitter follower, $C_L = C_{bc} + C_{cs}$, and $R_L = V_s/I_s$, inversely proportional to the switching current.

At very high currents, $\tau_d \propto F_{max}$, which reaches from an estimated maximum of 33 GHz for Si to 45 GHz for SiGe devices (cf. Fig. 11) Improvements in F_{max} are achieved with self-alignment schemes to reduce C_{bc} and C_{cs}, and can be further reduced by designing the device layout for minimum base resistance, i.e. long, narrow emitter stripes. The corresponding required current does not allow for high levels of integration however.

Instead, much better efficiency is obtained when the capacitive term $R_L \times (C_L + 2 \times C_{bc})$ is approximately equal to the profile contribution $(1 + R_b \times I_s/V_s)/2\pi f_T$. It can easily be seen that higher f_T at the expense of high base resistance and/or collector capacitance has minimal impact on circuit performance. The measurements on unloaded ring oscillators support this conclusion as shown in Fig. 12.

Minimum parasitic capacitances are even more important to reduce the power-delay product at low current. In this regime the performance of the vertical doping profile is no longer dominated by the base and collector transit times, but rather the specific junction capacitance is key to reduce power and delay. As discussed above, for the same basewidth delay, lower base-emitter junction capacitance can be obtained, to further improve the speed of ECL digital circuits.

Other Applications

For analog or other applications not limited by power, the designer can use the additional degree of freedom of the Ge profile more liberally to match the circuit performance to the intrinsic transistor profile capabilities. As expected from Equation (1), the f_T cut-off frequency has been shown (8) to increase from 75 GHz at room temperature to 94 GHz at liquid nitrogen temperature (cf. Fig. 13). Note that the speed of the Si devices also increased at low temperature, albeit only at extremely high current density. This trade-off between speed and current density is a fundamental difference between the various material systems for device operation. As can be seen in Figs. 1 and 14, SiGe achieves higher speed than Si (but less than InGaAs based HBTs for example) for a given current density, while higher profile speed through conventional scaling always requires higher current density. Due to the fact that a thinner base demands higher base doping, the base-emitter capacitance per unit area is increased. Thus a higher current density is required before the capacitive junction charging time equals the shorter base transit time (cf. Fig. 5). Since the collector doping should be designed to support this current density, it too has to be raised. This in turn increases the base-collector capacitance, which hinders circuit speed (see Equation (3)). Another important factor for analog applications, namely current gain, can be controlled independent of the base doping:

$$\frac{\beta(Si)}{\beta(SiGe)} \simeq \frac{\rho_{bi}(Si)}{\rho_{bi}(SiGe)}\, e^{-\Delta E_{g(BE)}/kT}\, \frac{kT}{\Delta E_{gG}} \qquad (4)$$

where $\Delta E_{g(BE)}$ is the bandgap reduction due to the Ge at the base-emitter depletion edge. This profile design flexibility allows for lower noise and higher Early voltage designs.
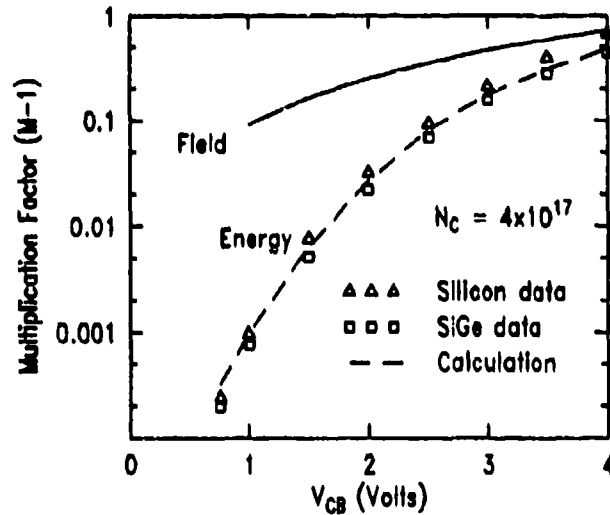

Figure 7 (ref 4)
Measured and calculated multiplication factors for Si and SiGe-base profiles using $\lambda = 80$ nm for the energy calculation.
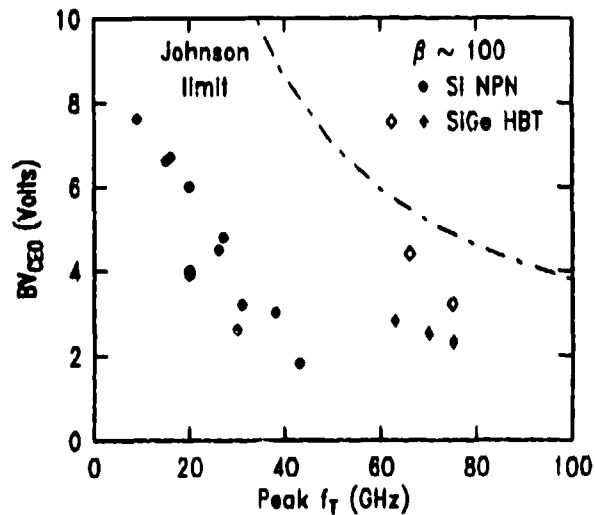

Figure 8 (ref 5)
Measured f_T and BV_{ceo} values illustrating the speed-breakdown trade-off for implanted and epitaxial Si base and SiGe base devices.
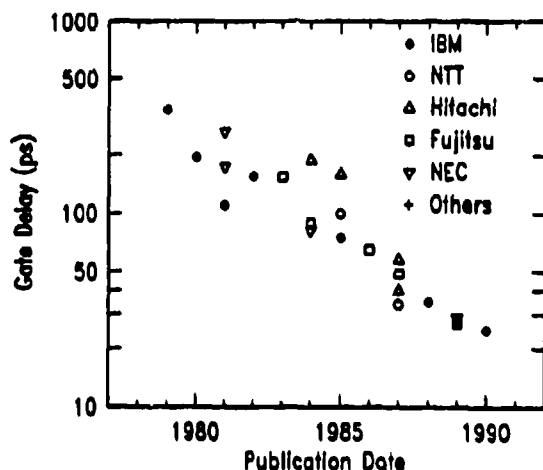
Figure 9
Reported unloaded ECL ring-oscillator speed
records versus year, showing a doubling
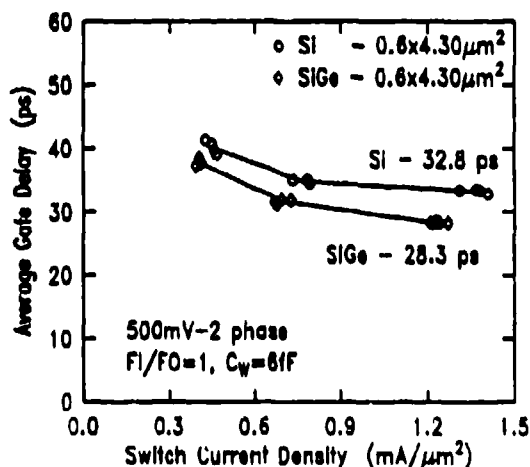about every three years.

Figure 10 (ref 5)
Comparison of ECL delay of Si and SiGe
transistors detailed in Table 1.

Discussion

The advantage of SiGe for profile design is that it
provides an extra degree of freedom to work within
the design constraints of base resistance, cut-off fre-
quency, and breakdown/leakage (9), since the base
transport time can be reduced without changing the
doping profile. The additional flexibility of device
optimization using Ge depends on the application.
Digital ECL logic has probably the least leverage,
but push-pull circuits are expected to benefit much
more from high f_T transistors. On the other hand,
it is clear that the even the intrinsic device potential
of SiGe HBTs is not as great as that of, for example,
AlGaAs-InGaAs HBTs, primarily because of the

Si-like electronic properties of low percentage SiGe
alloys. On the other hand, it is indeed the compat-
ibility with Si technology that makes SiGe technol-
ogy so exciting: an extra degree of freedom is
available to Si technology, allowing better device
design optimization and making inroads in applica-
tions which are out of reach for pure Si, while cap-
italizing on the vast technology base of Si
technology. However, the technology challenge of
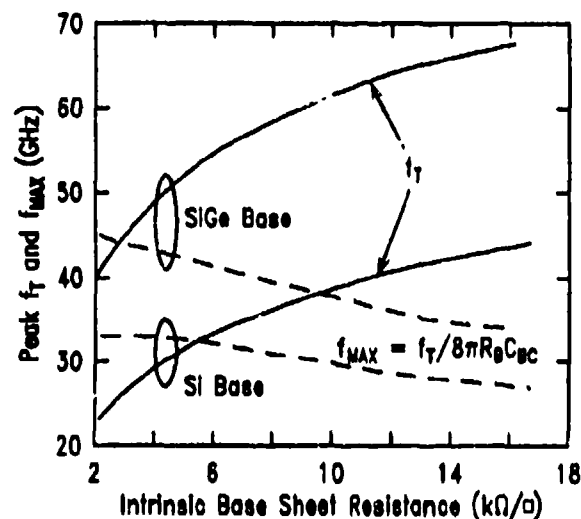integrating strained epitaxial-base devices into exist-

Figure 11 (ref 9)
Simulation showing f_T (solid lines) and
f_{MAX} (dashed lines) dependence on zero bias
intrinsic base resistance. The structure of the
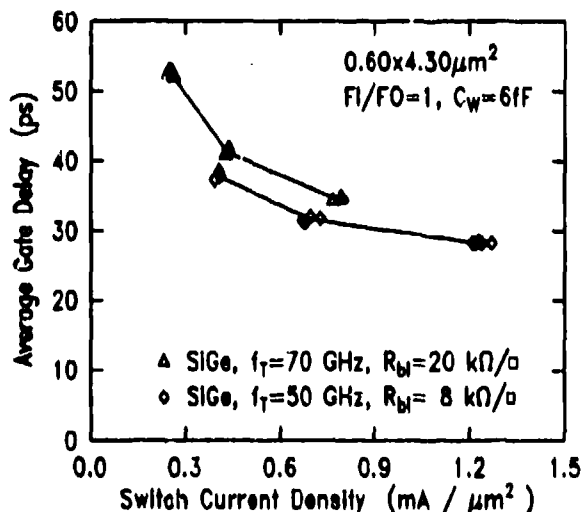devices detailed in Table 1 was assumed.

Figure 12
Comparison of ECL delay of "high" f_T-R_{bi}-
C_{bc} and "low" f_T-R_{bi}-C_{bc} SiGe devices. The
circuit performance with the higher f_T device
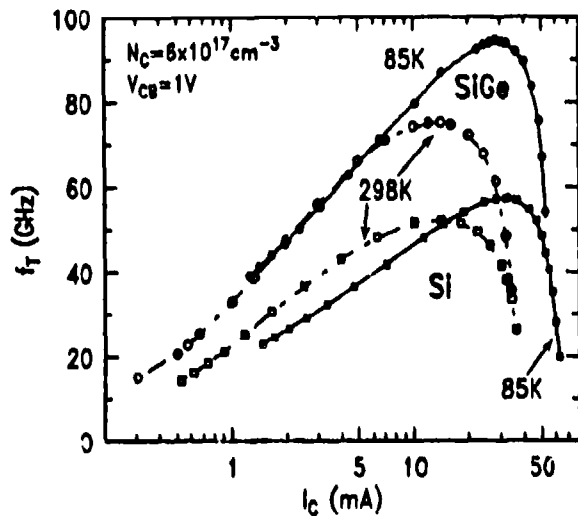is actually the slower of the two.

Figure 13 (ref 8)
Collector current dependence of f_T at 298K and 85K for Si and SiGe devices. In both cases, peak f_T and maximum current density increase with lower temperatures.
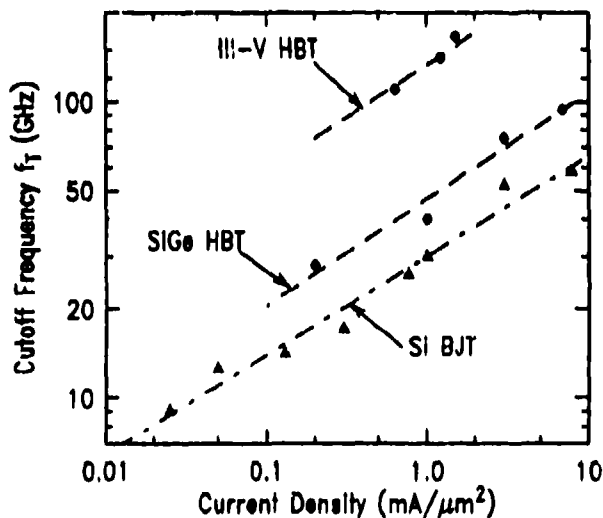

Figure 14
Reported record f_T versus current density comparing the intrinsic potential of III-V and SiGe HBTs with Si homojunction transistors.

ing processing techniques and achieving adequate control of all the critical parameters is an enormous engineering challenge.

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